REAL INTENT

Revolutionary Intent Driven Sign-off

True Multimode CDC Sign-off

Vikas Sachdeva

Real Intent Inc., Sunnyvale, CA

I. INTRODUCTION

Over the past decade, the shrinking of process technologies has dramatically increased the amount of logic in a single chip. Typical System-on-Chip (SoC) designs integrate functionality that was part of many discrete chips earlier. SoC designs today have many subcomponents with varying degrees of complexity and configurability. This increased complexity and configurability in SoCs translates to a large number of operating modes and scenarios. Accompanying this abundance of operating modes, there is a proliferation of internal and external protocols and aggressive power requirements that lead to an explosion in the number of asynchronous clocks in the SoC. Figure 1, shows how SoC designs have evolved over the last decade.

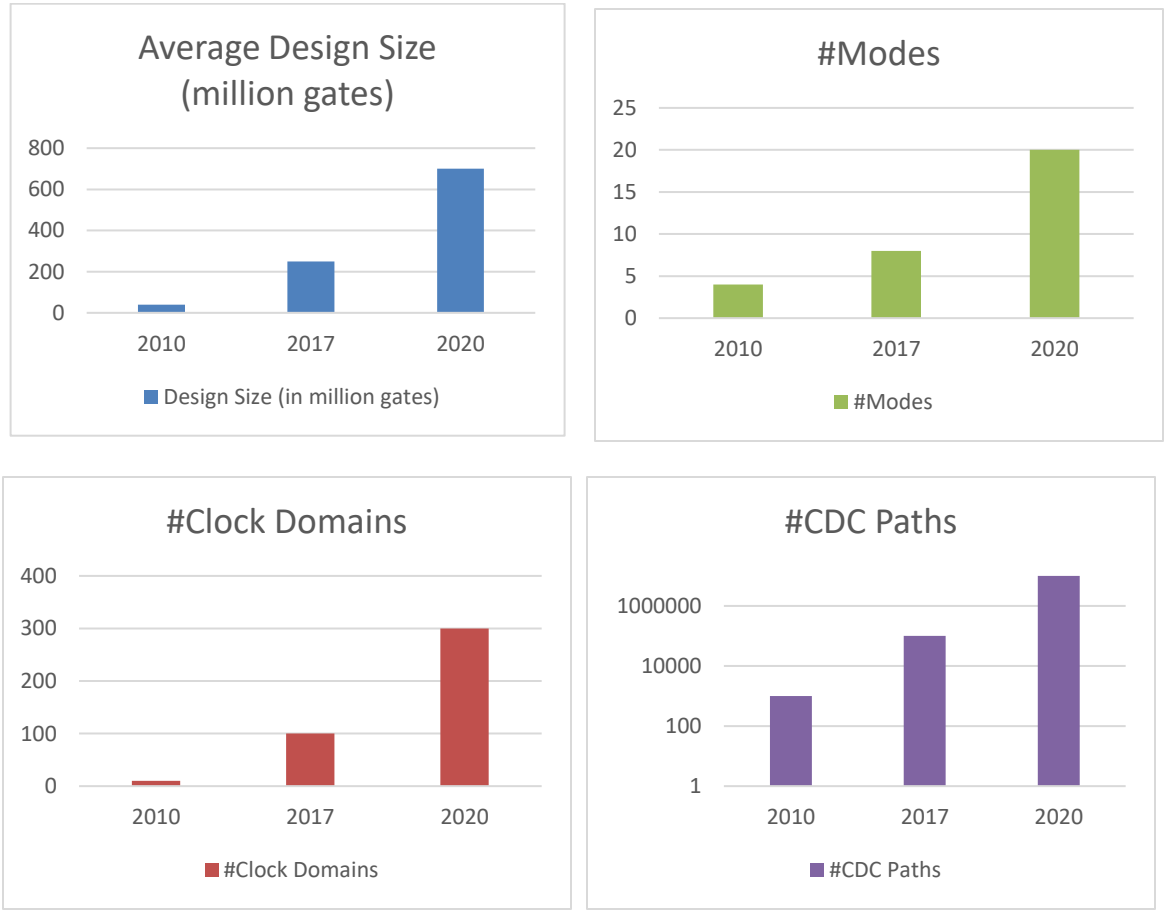

Figure 1: Evolution of SoCs in this decade

Ensuring that these complex SoCs work according to specifications, in all operating modes with numerous asynchronous clock interactions, is an incredibly challenging problem being faced by design and verification engineers across the globe.

This paper starts by discussing typical approaches designers take currently to verify Clock Domain Crossing (CDC) aspects of these complex SoCs. It then elaborates on some of the risks associated with these approaches. Following that, it creates a set of requirements for a

CDC verification tool that can mitigate these risks and enable True Multimode CDC sign-Off. In the final section, the paper introduces Verix CDC, a multimode CDC verification tool that addresses all these requirements and enables a comprehensive multimode CDC Sign-off methodology for these complex SoCs. For more information on CDC analysis in general, refer to “Clock Domain Crossing Demystified: The Second Generation Solution for CDC Verification” on the Real Intent website. (www.realintent.com/white-papers/)

II. Current CDC Methodology for Multimode SoCs

The growing complexity of designs has led to a design productivity crisis, Multimode designers are faced with the conflicting demands of doing comprehensive CDC sign-off and meeting tape-out deadlines. Let’s consider some typical approaches designers take to sign-off on multimode CDC, and the risks and challenges associated with each.

CDC analysis on worst-case mode(s)

In order to balance chip schedules with comprehensive sign-off, designers often pick one or more modes that are believed to be representative of worst-case CDC analysis. The assumption is that if CDC is signed-off on these modes, then the remaining operating modes will also be clean. This approach comes with the following risks and challenges:

- Identifying and creating worst-case modes requires deep design and architecture knowledge and is prone to manual errors
- It may not be possible to create a few worst-case modes that cover all chip operating scenarios
- Signing-off on selected modes does not guarantee safe chip operation on all modes
- CDC issues can slip through in this approach and cause silicon failures, or late discoveries in netlist simulations can impact tape-out schedules.

CDC analysis on all individual modes

Another approach is to sign-off CDC in each of the individual modes. Parallel computing and advances in hardware technology today allows designers to take this approach. But this approach comes with its own challenges and risks. Some of those are listed below:

- The manual effort to set up each of the individual modes for CDC analysis can be very time consuming, and is error prone because modes can be missed
- The approach does not help reduce the manual effort of reviewing the analysis results across all the different modes
- Fixing a CDC issue in one mode can introduce a CDC problem in another mode, so the whole process can be very iterative
- The huge iterative effort required in this manual and error prone approach can impact tape-out schedules

III. Requirements of the Multimode CDC Methodology

The previous section talked about the challenges and risks associated with multimode methodologies currently in use by designers. Using these as a basis, this section presents a set of requirements for a robust and efficient multimode CDC sign-off methodology.

The ultimate goal of any CDC methodology is that it needs to ensure that all possible CDC violations are found, i.e. that it is complete. In multimode, as the amount of CDC analysis data can increase manifold, the methodology not only needs to report all possible CDC violations but also needs to present information in such a way that it leads to efficient CDC sign-off. The high-level requirement is to enable users to complete a comprehensive CDC sign-off in multimode without risking tape-out deadlines. This can be enabled if the following features are enabled in the methodology:

Clocks and clock-relationship intent

In single-mode analysis, as only one clock can reach one flop, the crossing path is either synchronous or asynchronous depending upon whether clocks reaching the flops are synchronous or asynchronous. In multimode, when multiple clocks can reach one flop, the same crossing path can be synchronous or asynchronous depending upon what clocks are selected for analysis.

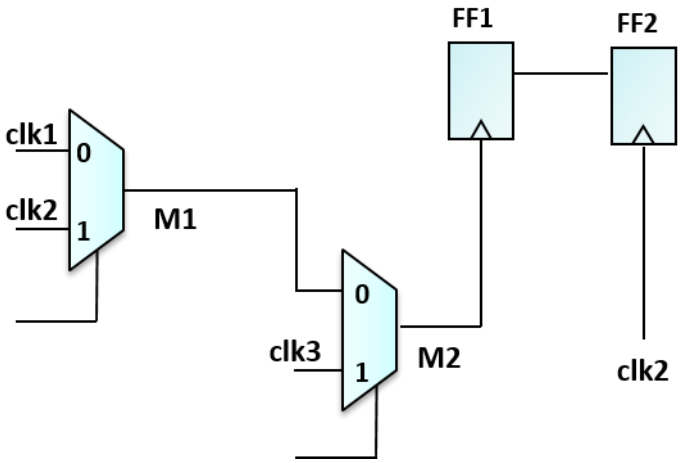

Figure 2: CDC crossing depending upon clock selection

For example in Figure 2, assuming `clk1`, `clk2` and `clk3` to be asynchronous, the path from `FF1` to `FF2` can be synchronous if `clk2` is selected to reach `FF1`, and asynchronous if `clk1` or `clk3` is selected to reach `FF1`.

Also, in the multimode context it is possible that all clocks are defined in the same constraints file, but belong to different modes of the design, and therefore do not interact in any CDC crossing.

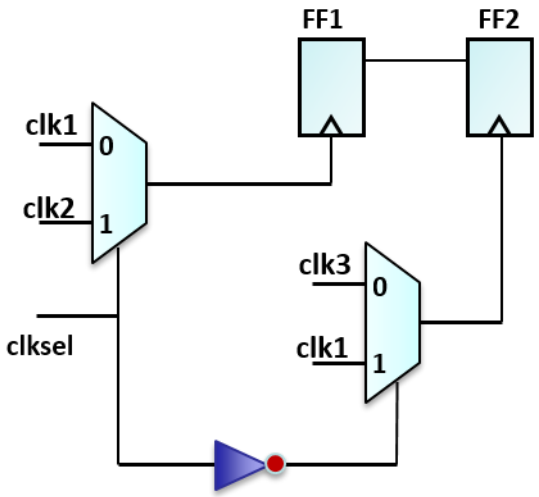

Figure 3: Clock exclusivity based upon clock selection logic

For example in Figure3, all clocks `clk1`, `clk2` and `clk3` are defined in the constraints file, but looking at the clock selection logic one can deduce that when `clk1` reaches `FF1`, `clk3` cannot reach `FF2`, and hence there is no CDC crossing involving `clk1` and `clk3` in this circuit. Only `clk2` and `clk3` create a CDC crossing.

These examples clearly indicate that in order to accurately represent design intent for multimode CDC, just synchronous or asynchronous clock relationships are not sufficient. We need additional relationships like clock exclusivity. Clocks can be exclusive all across the design (e.g. a scan-test clock and a functional clock), or they can be exclusive in a certain portion of the design (e.g. low-power clocks for processors on mobile chips). Clocks can also be exclusive not just because of clock-selection logic, but also because of clock-generation logic.

The implication from the above is that clock intent plays a major role in multimode CDC analysis. Hence, for an accurate multimode CDC methodology, it is imperative to automate the inference and interpretation of the underlying clock intent in the design. Otherwise the user will end up debugging issues of no consequence. Also, the user should be able to provide architectural clock intent assumptions to further improve the efficacy of the analysis.

CDC Intent in multimode context

For accurate CDC analysis, the CDC tool not only needs to identify each crossing path in the design, but also to deduce functional correlation between these paths.

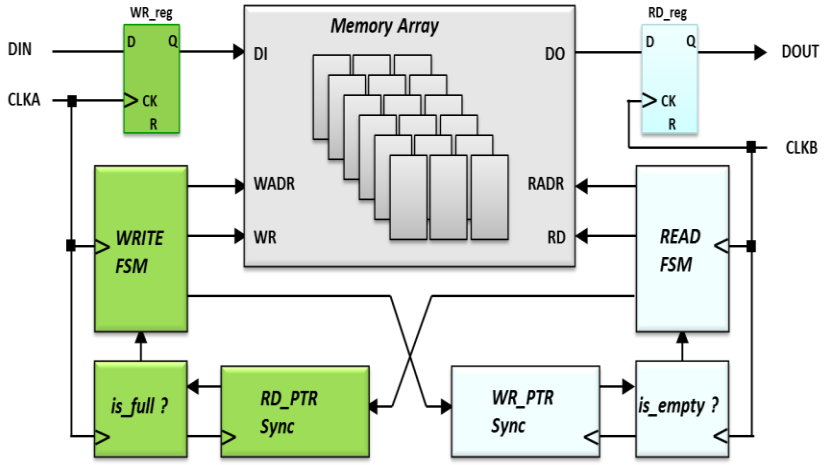

Figure 4: FIFO based synchronization

For example consider the FIFO-based synchronization scheme shown in Figure 4. There are the following three CDC paths in this circuit:

- Memory Array to Read register (`RD_reg`)
- READ FSM to Synchronized Read Pointer (`RD_PTR`)
- WRITE FSM to Synchronized Write Pointer (`WR_PTR`)

Synchronized Read and Writer pointers above are used to generate FIFO full (`is_full`) and FIFO empty (`is_empty`). FIFO-based synchronization works correctly only when Read/Write pointers are appropriately synchronized and FIFO full & empty signals are properly generated. This requires the tool to do a deeper functional analysis on the top of identifying CDC paths to correctly classify a CDC path as good or bad.

In multimode, the analysis not only needs to interpret underlying functional intent for accuracy, but also needs to take a holistic view of all modes to reduce the volume of CDC data. Simplistic analysis here can lead to hundreds of thousands of crossings to be reviewed for typical designs.

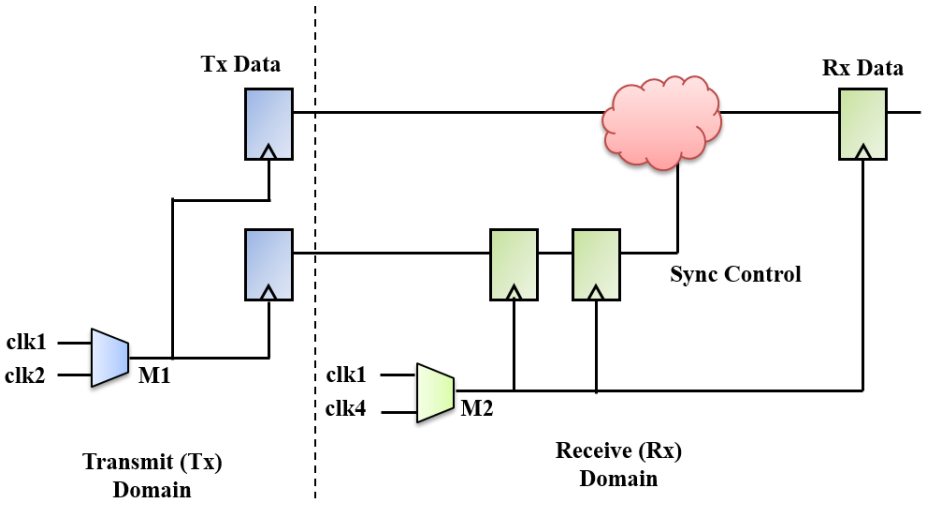

Figure 5: Mux-based synchronization scheme

For example, refer to Figure 5, which shows a mux-based synchronization scheme. In certain modes, when `clk1` is selected in both `M1` and `M2`, the `Tx-Data` to `Rx-Data` path will be synchronous. When other clocks are selected, the same path can be asynchronous and the structure should be identified as being correctly synchronized.

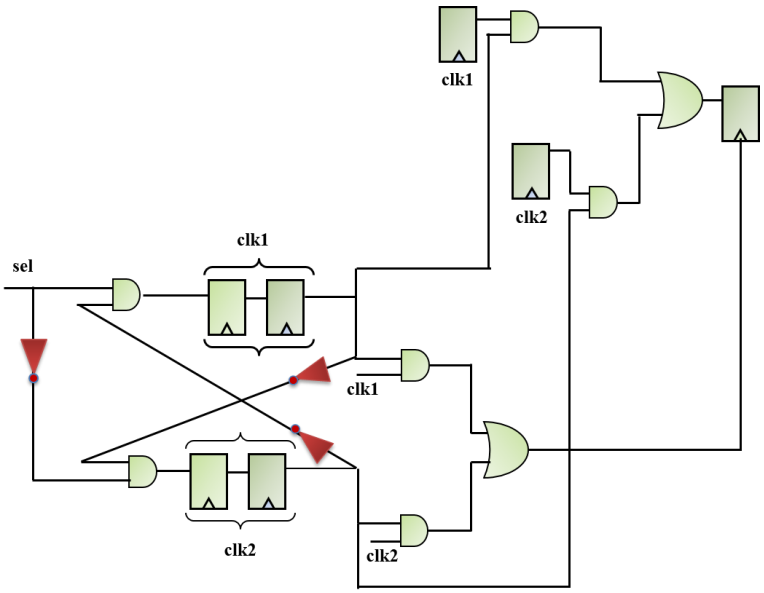

Figure 6: Dynamic clock switching between asynchronous clocks

Consider a more complex case as shown in Figure 6 where two asynchronous clocks `clk1` and `clk2` are present in the design, and the design can dynamically shift from `clk1` to `clk2` without introducing a CDC problem in the design.

The examples show that in multimode it is very important for the tool to interpret the CDC intent of the design so as to not report bogus violations. In scenarios when CDC design principles are not met in multimode, it is equally important for the CDC tool to report the violation in such a way so that the data can be efficiently reviewed and managed. Simplistic reporting can lead to copious amounts of data and unnecessary reviewing, which can delay chip schedules.

Efficient debug

Efficiency of debug is an important aspect of any CDC methodology. In multimode the efficiency challenge is magnified because a CDC violation can occur due to a number of different clock and data path configurations. To achieve the high-level goals of comprehensive sign-off without delaying tape-out schedules, the CDC methodology in multimode should be able to provide violation-specific debug to effectively root cause and fix problematic data-paths and clock-paths in the design.

IV. Summary of Requirements for Multimode CDC Methodology

The previous section explained the challenges in multimode CDC verification. With that as the basis, the following items can be considered to be the requirements of a multimode CDC verification tool and methodology for scalability and sign-off level confidence:

- Manage and interpret clocks and clock relationships
- Deduce CDC intent in multimode context
- Report CDC violations taking holistic view of all modes
- Efficient debug

V. True Multimode CDC Verification with Verix CDC

Verix CDC, Real Intent's revolutionary first-to-market multimode CDC sign-off solution, enables an efficient sign-off-quality multimode CDC verification. Built on proprietary ***static-intent verification*** technology, ***Verix CDC*** can interpret clock and clock relationship intent. It can automatically deduce exclusive clock-modes, and exclusive clock-regions in the design. It also automatically understands the underlying CDC intent in multimode to provide accurate and comprehensive results.

Verix CDC only requires a single setup, even with multiple possible modes in the design. Based on this setup, ***Verix CDC*** analyzes the design with a holistic view of all the modes in the design. After the analysis is done, the tool ensures that only one violation is reported for one CDC issue in the design, even though the problem may be present in more than one mode in the design. This provides an unprecedented runtime and productivity boost for multimode designs, saving weeks of sign-off effort. It also ensures that when a CDC issue is fixed for one mode, the user doesn't have to iterate through all the other modes to see how they are affected.

In addition to all the above, ***Verix CDC*** supports an integrated visualization tool. The ***iDebug*** GUI provides pruned annotated schematic and source views that focus on the faulty logic. The schematic generated is tuned to the specific CDC problem being reported. For example, Figure 7 shows the schematic for glitch violation in ***Verix CDC***.

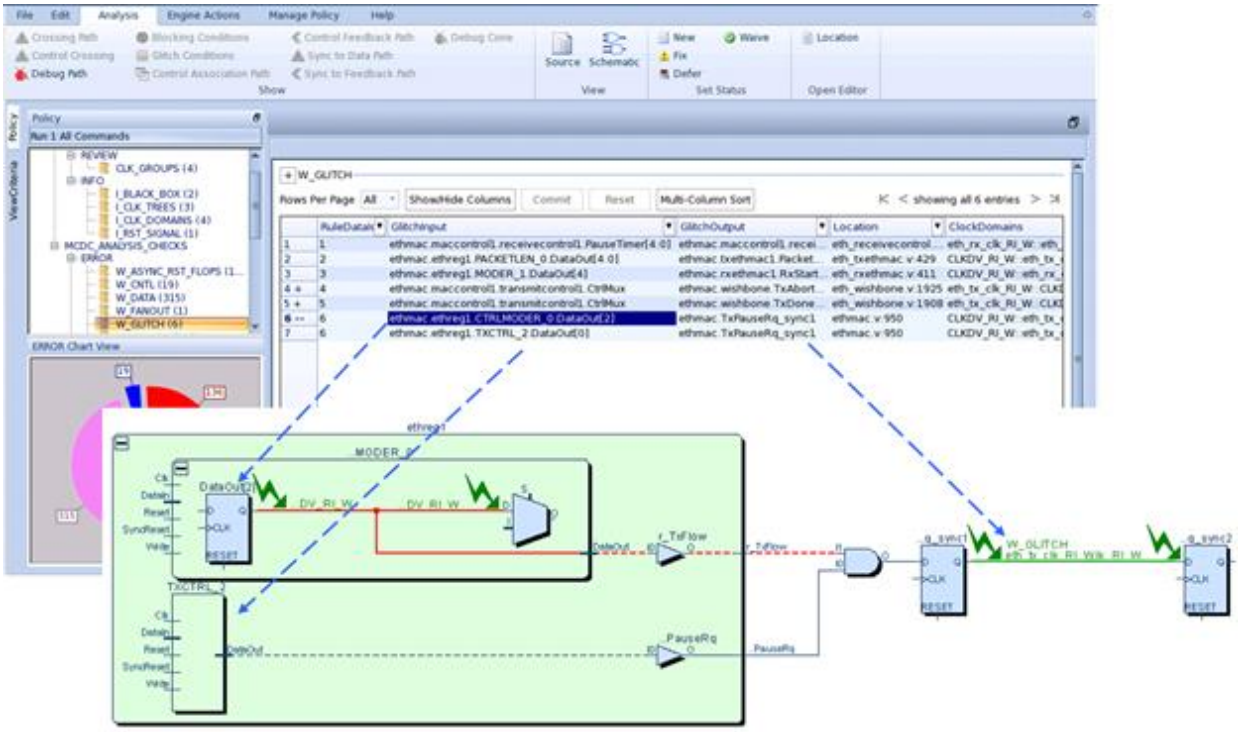

Figure 7: Pruned annotated schematic in iDebug

iDebug interprets the debug information generated by Verix CDC, and with a few mouse clicks, users are directed to associated data-path, clock-path or clock combinations that are causing CDC violations. (See Figure 8)

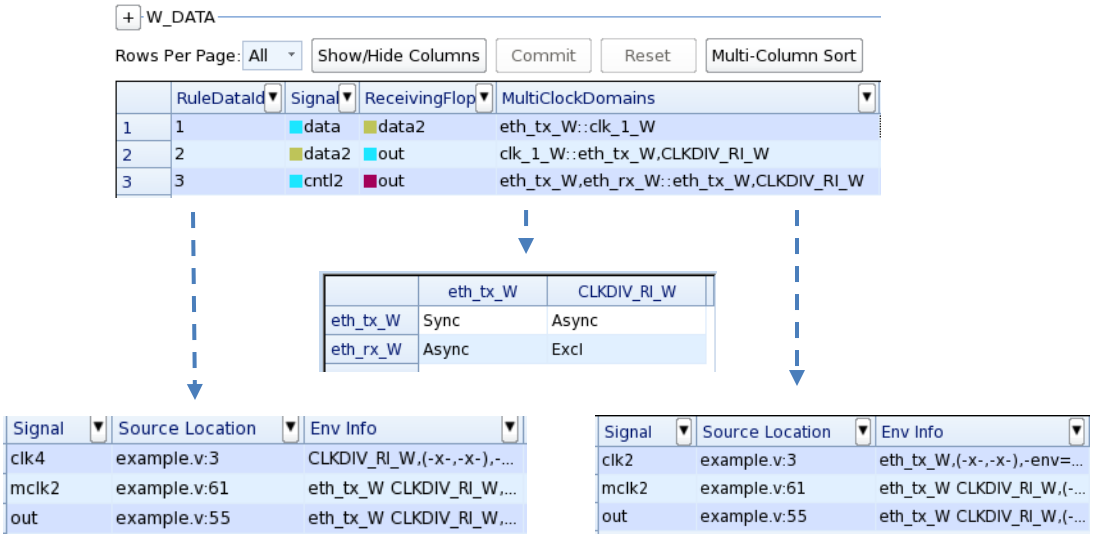

Figure 8: Context specific multimode debug in iDebug

In addition to the above, schematics are annotated with CDC attributes specific to the problem being investigated. These attributes enable context-specific root-cause analysis, and allows users to quickly identify sources of clocks, resets, constants and other CDC properties in the design. Users can efficiently investigate CDC problems deep in the design to quickly root cause for any CDC warnings or errors. At every step in the debug, ***iDebug*** provides helpful guidance and suggests actions to enable users to pinpoint the source of the problems quickly.

All these features, enabled by the ***static intent verification*** technology of ***Verix CDC,*** very efficiently solve the multimode CDC sign-off problem being faced by designers working on modern SoCs. Using ***Verix CDC***, designers can comprehensively sign-off across all modes using a single setup without risking chip tape-out schedules i.e. do a True Multimode CDC sign-off.

VI.SUMMARY

With shrinking process technologies, design teams are integrating much more logic in a single SoC. The increased logic often comes with enhanced configurability. In addition to this, there is a proliferation of internal and external protocols and aggressive power requirements that lead to an explosion in the number of asynchronous clocks. Ensuring that these complex SoCs work according to specifications, in all operating modes with numerous asynchronous clock interactions, is an incredibly challenging problem being faced by design and verification engineers across the globe. A multimode CDC flow that can accurately and efficiently automate CDC analysis across all modes can solve the sign-off challenge being faced by CDC designers working on these SoCs.

Verix CDC's proprietary *static intent technology* automates the multimode flow to reduce manual effort. ***Verix CDC*** can interpret clock and CDC intent in multimode context, which is key to accuracy, and to prevent designers from debugging non-issues. It can automatically deduce non-operational clock modes, and analyze exclusive clock-regions in the design. ***Verix CDC*** has a holistic view of all modes in the design. It requires a single setup, even with multiple modes in the design. This provides an unprecedented runtime and productivity boost for multimode designs, saving weeks of sign-off effort. On top of that, ***Verix CDC*** saves debug time by avoiding the iteration and duplication of reviews. It also enables context-specific debug, tuned specially for multimode analysis. The ***Verix CDC*** multimode flow was developed with several partners who have helped refine the presentation of violations, and to ensure that the tool provides appropriate debug information for the user to understand the cause and effect of a violation. ***Verix CDC's*** proprietary ***static intent verification*** technology delivers **True Multimode CDC sign-off.**

REFERENCES

[1] http://www.realintent.com/real-intent-products/verix-cdc/

2017-05-23, v1

REAL INTENT

Revolutionary Intent Driven Sign-off

Real Intent, Inc.
990 Almanor Avenue, Suite 220
Sunnyvale, CA 94085
support@realintent.com
Phone: 408-830-0700
Fax: 408-737-1962

realintent.com