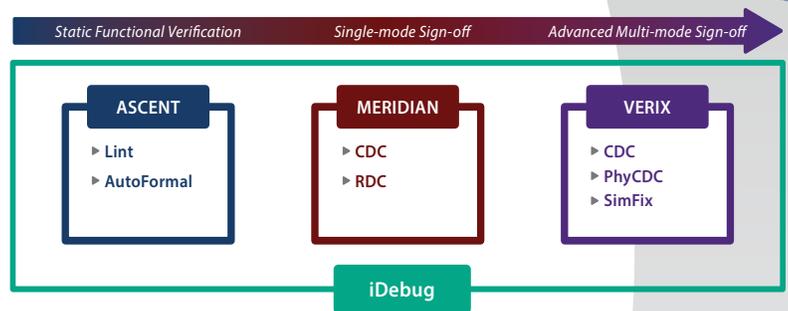


## Real Intent Product Overview

Real Intent is the leading provider of EDA software to accelerate Early Functional Verification and Advanced Sign-off of digital designs. It provides comprehensive clock-domain crossing verification, advanced RTL analysis and sign-off solutions to eliminate complex failure modes of SoCs. The Verix, Meridian, and Ascent product families lead the market in performance, capacity, accuracy and completeness.

### Real Intent Product Families

Real Intent offers three product families—Ascent for early functional verification before synthesis, Meridian for advanced sign-off verification not possible with simulation or static timing analysis, and Verix for true multimode sign-off verification unlike anything else in the market.



### Ascent for Early Functional RTL Verification

**Ascent Lint** is the industry's fastest and lowest-noise RTL lint solution. It includes smart rules that perform syntax and semantic checks for today's complex System-on-Chip (SoC) designs. **Ascent Lint** is unique in the industry in terms of delivering high capacity, comprehensiveness and ease of debug.



**Ascent AutoFormal** builds on **Ascent Lint** to find elusive bugs in RTL. It performs comprehensive verification using automatic check formulation followed by deep-sequential formal analysis. **Ascent AutoFormal** can improve verification efficiency substantially and detect up to 50% of design functional errors prior to testbench development and simulation. It is the only automatic formal tool with root cause analysis, drastically reducing the debug time and the number of iterations necessary to get to functional closure.

### Meridian for Clock and Reset Sign-off Verification

**Meridian CDC** is the fastest, highest capacity and most precise CDC solution in the market. It performs comprehensive structural and functional analysis to ensure that signals crossing asynchronous clock domains on ASIC, or FPGA devices are received reliably. With giga-gate capacity, **Meridian CDC** is the only solution that enables all aspects of CDC sign-off.



**Meridian RDC** is the fastest and most precise reset domain crossing sign-off tool in the market. It performs comprehensive static analysis to ensure that signals crossing reset domains work reliably. Among other things, Meridian RDC identifies metastability problems arising from software and/or low power resets. Meridian RDC is the only solution that enables comprehensive reset domain crossing sign-off.

## Verix for Advanced Multimode Sign-off Verification

**Verix CDC** is the most precise multimode CDC solution in the market, specially architected for multimode analysis with static intent verification. It performs comprehensive CDC analysis with multiple clocks reaching the flops, allowing all possible scenarios to be covered in a single run. It is built on specialized technology that statically infers clock relationships to enable the comprehensive clock-intent management and true multimode CDC sign-off.



**Verix PhyCDC** is the only solution that delivers comprehensive netlist CDC sign-off including glitch checking. RTL CDC sign-off assumptions may become invalid because of logic synthesis and power optimizations. **Verix PhyCDC** performs comprehensive structural and functional analysis to ensure that signals crossing asynchronous clock domains are CDC-safe at the gate-level. Complementing Real Intent's **Verix CDC** solution that provides comprehensive analysis for RTL sign-off, **Verix PhyCDC** delivers the most advanced netlist sign-off for giga-gate designs.

**Verix SimFix** the Verix X-Pessimism correction system, enables accurate gate-level simulations (GLS) that are necessary for a thorough verification sign-off. **SimFix** uses mathematical methods to identify conditions under which pessimism can occur, and to determine the correct value when those conditions occur. It then generates files that, when used in simulation, will detect and correct pessimism so that the simulation accurately models real hardware.

## Common Infrastructure

**iDebug** is the state-of-the-art debugging environment for its suite of products for the verification of digital designs. **iDebug** provides an intuitive debugging experience that is universal across all Real Intent tools. It employs a database for the intelligent hierarchical analysis of design intent. It includes an integrated visualization capability, **iVision**, that provides design source browser, schematic and waveform visualization. The intent analyses of **iDebug** distinguish the root cause of issues, and minimize iterations and debug time, enabling powerful sign-off mechanisms. Now with Intent Wizard, context-specific intent and design debug guidance that cuts the intent and sign-off debug time by half.



Revolutionary Intent Driven Sign-off

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