

Multimode Intent Driven Clock Domain Crossing Sign-off

Verix CDC is the most precise multimode CDC solution in the market, specially architected for multimode analysis with static intent verification. It performs comprehensive CDC analysis with multiple clocks reaching the flops, allowing all possible scenarios to be covered in a single run. It is built on specialized technology that statically infers clock relationships to enable the comprehensive clock-intent management and true multimode CDC sign-off.

Why Multimode?

Current single-mode methodology for CDC sign-off uses SDC constraints with case analysis for each mode. That necessitates the reviewing of CDC issues in each mode separately and several iterations to ensure that all modes are clean. With the rapid rise in the number of modes, it is nearly impossible to sign-off each mode individually. In addition, static timing analysis, traditionally done in single mode, has already moved toward multimode analysis. As a result, multimode SDC is more readily available to start multimode CDC signoff.

In single-mode CDC sign-off, multiple runs of CDC analysis are needed for sign-off. As shown in *Figure 1*, the data crossing from *FF1* to *FF2* will be reported only if *sel* is set to 0. In multimode, CDC signoff can be achieved in a single CDC run. No clock selection through *sel* is needed and the data crossing from *FF1* to *FF2* will be reported.

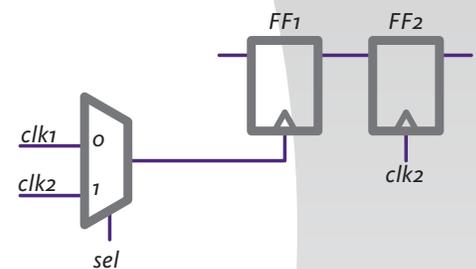


Figure 1. Multiple clocks feed into the flops

Multimode CDC Sign-off

Verix CDC, with its proprietary static intent verification technology, is the most precise and lowest-noise solution in the industry for multimode CDC analysis. The CDC analysis is performed using multiple clocks reaching the flops. SDC constraints are applied without mode select, allowing multiple clocks to propagate to the flops. It verifies all the paths that are not timed in STA, so no crossings and violations are missed. Verix CDC can functionally analyze clocking logic to interpret clocking scenarios that are not logically possible in the design. In addition users can provide further clock-architecture level information to improve functional analysis.

Static Intent Verification

The specially designed static intent verification technology is the foundation for multimode CDC analysis. In multimode, since all clocks are enabled together for the analysis, it is imperative to infer the underlying clock intent in the design, for the tool to be accurate and low noise. Static intent verification technology can automatically deduce whether certain clock interactions are not possible in certain logic areas of the design. The technology infers and applies the logical and graphical relationships between clocks to enable clock intent verification.

Multimode Intent Management and CDC Debug

Verix CDC's multimode reporting keeps users focused on important multimode CDC analysis issues through an efficient organization of the results of the analysis. Helpful guidance and suggested actions help users pinpoint the source of the problems quickly. Real Intent's state-of-the-art design-intent debugger and analysis manager—iDebug—provides for user configurability and programmability with its command-line interface (CLI).

Verix CDC supports an integrated visualization tool. Annotated and pruned schematic views focus on fault-related logic, and with a few mouse clicks, users are directed to the RTL source code that caused the problem. This debug approach allows for easy investigation deep into the design to isolate the root cause for any warnings and errors. As shown the *Figure 2*, the CDC violations are reported with multiple interacting clocks. Users can view further details and the in-context schematics.

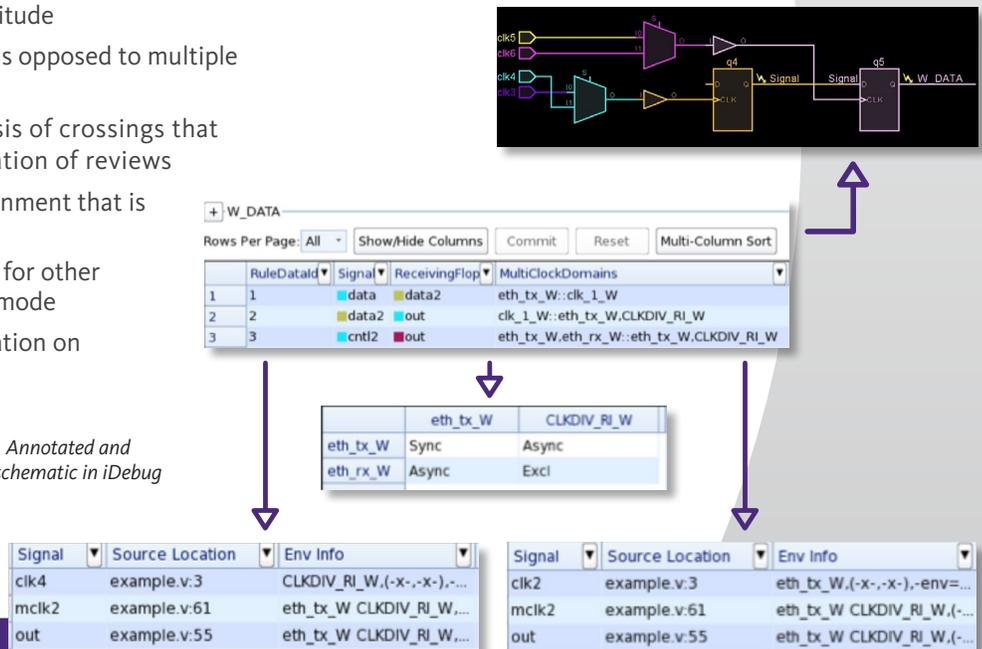
Features

- Most precise multimode CDC reporting—no crossing missed
- Static intent verification technology provides unprecedented precision, ease of use, and debug
 - *Application-dependent specification of intent*
 - *Separation of logical and physical attributes—easy to manage, review, refine*
 - *Automatic graphical and logical inheritance*
 - *Context-aware management when moving from block to top or vice versa*
 - *Ensuring intent is consistent, complete, correct, and easy to refine and review*
- Graphical and schematic based review and debug—information presented in layered manner

Benefits

- Reduces runtime by an order of magnitude
- Requires single setup for multimode as opposed to multiple setups for individual modes
- Saves debug time by avoiding analysis of crossings that cannot occur, iterations, and duplication of reviews
- Enables a more intuitive debug environment that is tuned for multimode analysis
- Saves the need for iterative CDC runs for other modes after fixing CDC issues in one mode
- Highest capacity enables CDC verification on billion-gate SoC designs

Figure 2. Annotated and pruned schematic in iDebug



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