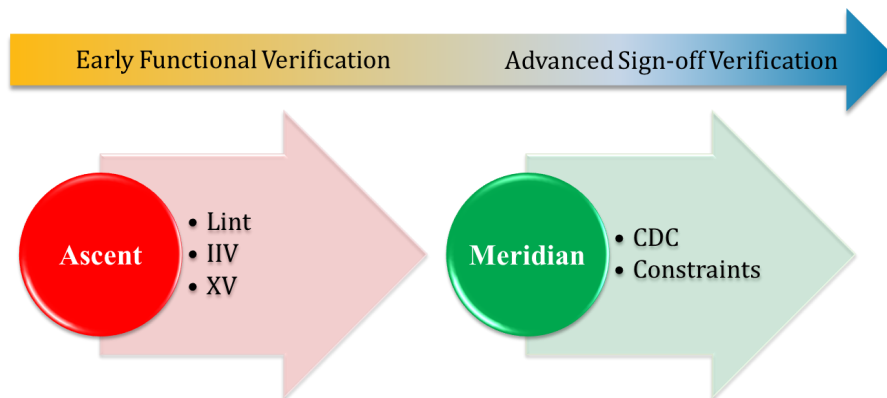


Ascent Lint is the industry's fastest and most accurate RTL lint solution. It includes smart rules that perform syntax and semantic checks for today's complex System-on-Chip (SoC) designs. Ascent Lint is unique in the industry in terms of delivering high capacity, comprehensiveness and configurability.

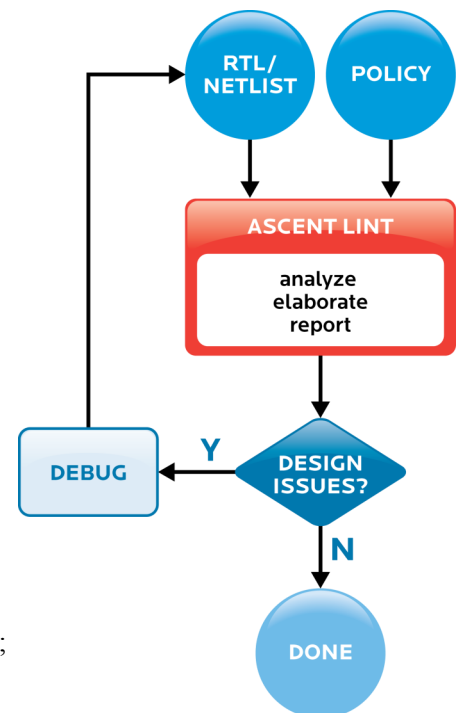


## BENEFITS

- Detects complex design bugs early in the design flow
- Finds design and coding guideline bottlenecks that impact simulation, synthesis, testability, and implementation costs
- Offers easy adoption, use and customization
- Integrates with Real Intent's tools and plugs straight into standard EDA flows
- Helps geographically dispersed design teams to create higher quality designs
- Offers high return on investment

## FEATURES

- Highest performance of any lint tool in the industry
- Low-noise, yet comprehensive violations report
- Fast and powerful debugging capability with cross probing to RTL design source; pinpoints the exact source of issues
- Offers rules from STARC Verilog and VHDL Policy, Verilog and System Verilog Gotchas, Reuse Methodology Manual, Principles of Verifiable RTL Designs, DataPath Synthesis rules, and rules based on Real Intent industry expertise
- Provides GUI for rule selection, waiving, and customization as well as debugging the violations report



Please visit [www.realintent.com](http://www.realintent.com) for more information.

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## ADVANTAGES

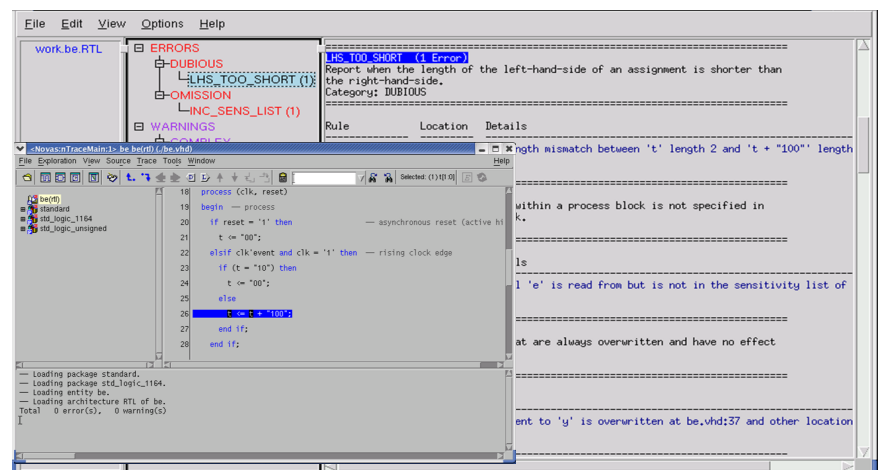
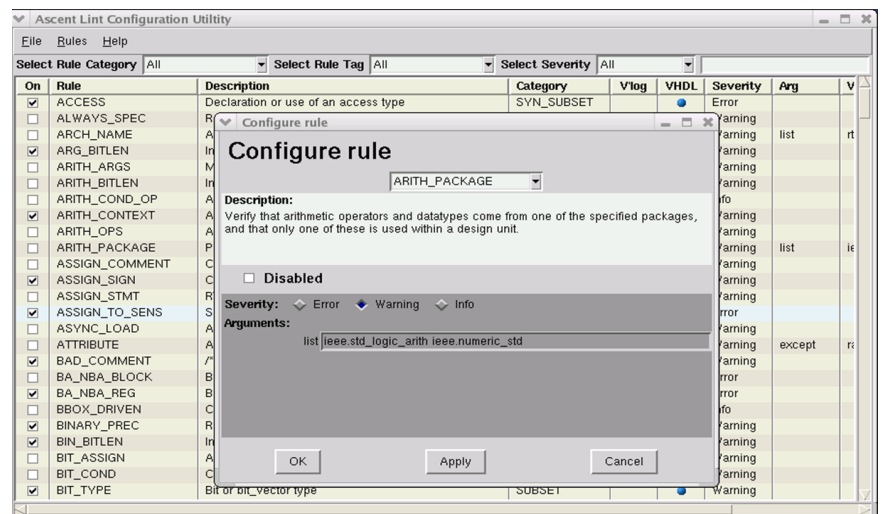
### Smart Rules

Ascent Lint offers smart Verilog, VHDL, and Netlist rules that detect design issues in the following areas:

- Legal but dubious modeling indicating probable errors
- Differences between simulation and synthesis semantics
- Naming and RTL coding conventions
- Subset restrictions to enforce modeling clarity and reduce complexity
- Opportunities to improve simulation performance
- Operations with hidden or expensive implementation costs
- Downstream tool flow issues
- Network and connectivity checks for clocks, resets, and tri-state-driven signals
- Module partitioning rules
- Testability

### Powerful GUIs

- Ascent Lint lintconfig is a graphical user interface that enables the user to configure and customize rules to create custom lint policies.
- Ascent Lint lintdebug is a graphical user interface that enables debugging of the lint report. With a few mouse clicks, it directs users to the violations, and cross probes to the exact source of the problem in the design source code, and schematic. It also provides editing design source files, rule re-configuration, and waiving right from the violation line. The lintdebug GUI also allows re-running lint analysis for fast turnaround time. The Ascent Lint debugger is integrated with SpringSoft's Verdi™ Automated Debug System which is available direct from Real Intent.



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