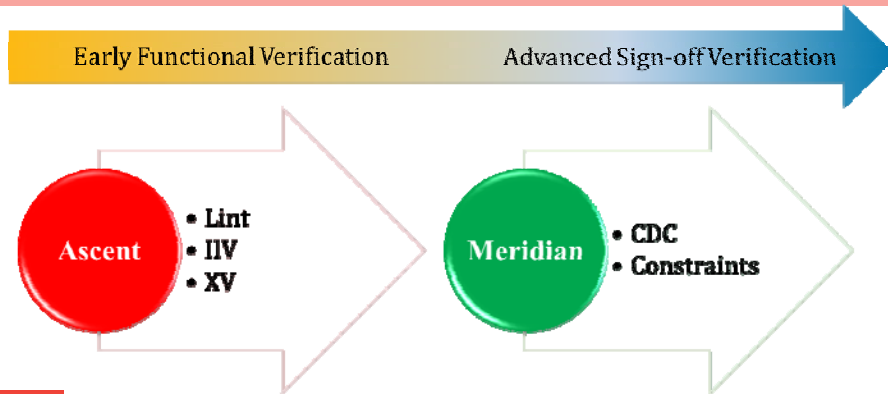


Ascent Implied Intent Verification (IIV) is an early functional verification tool that provides immediate return on investment by quickly finding elusive bugs in the RTL. Ascent IIV performs comprehensive verification using automatic check formulation followed by deep-sequential formal analysis. Ascent IIV can improve verification efficiency substantially and detect up to 50% of design functional errors prior to testbench development and simulation.

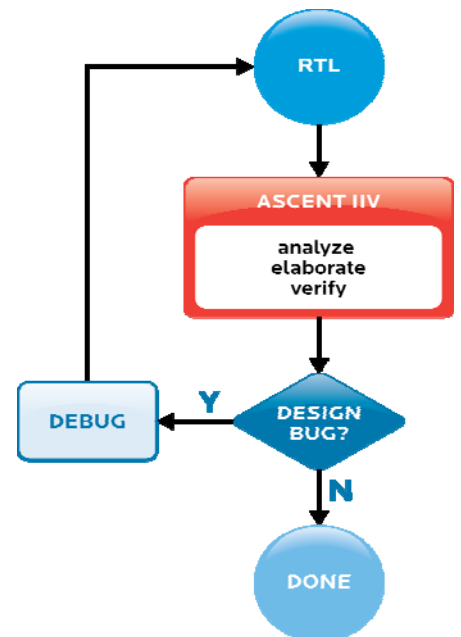


BENEFITS

- Powerful sequential formal analysis quickly finds common functional errors in the design especially in early RTL stage
- Start analysis long before simulation can start
- Easy to use, easy setup and intuitive methodology
- Provides sufficient block level verification that longer cycles of chip level verification are avoided
- Verifies designs with complex state machines

FEATURES

- Convergence Formal Engine™ provides highest capacity and performance
 - Provides full counter-examples in VCD format
- Fully automatic, requires no testbenches
- Leading-edge language support for VHDL, Verilog, SystemVerilog, and mixed languages
- Supports SystemVerilog SVA/VHDL PSL as constraints to improve accuracy of formal analysis
- Comprehensive analysis and reporting
- Root cause analysis minimizes debug!
- Easily integrates with Real Intent's tools and plugs straight into standard EDA flows



Please visit www.realintent.com for more information.

Real Intent, Inc.
505 N Mathilda Ave, Suite 210
Sunnyvale, CA 94085 USA
support@realintent.com
Phone: 408-830-0700
Fax: 408-737-1962



ADVANTAGES

Automatic Implied Intent Verification

Why wait for the design to be completely assembled and verify at the chip level with its inherent complexity? Automatic verification can start at the block level with no testbench development, and find bugs immediately. Waiting to the chip level to discover these bugs will leave you in a debug nightmare. Ascent IIV full sequential analysis can catch bugs earlier, driving the cost/bug down, and speeding the verification process.

Ascent IIV performs automatic implied intent verification to catch functional errors such as dead code, state machine deadlocks, synthesis pragma violations, etc. It analyzes the RTL and for every applicable instance of a particular design construct, it automatically generates assertions and instruments the RTL under test. It then performs formal analysis of these assertions that fall into one of the following two categories:

- **Undesired Sequence Check:** Assertions that ensure undesired behaviors are not present in the design. A VCD is provided that shows the sequence of inputs that can lead to the failure.
- **Desired Sequence Check:** Assertions that ensure desired behaviors are present in the design

Ascent IIV offers automatic functional error detection in the easiest to use methodology.

Automatic Incremental Capability

The Resume Verification facility saves considerable run time by enabling Ascent to continue from the exact internal state of a previous run.

Powerful Debugging Graphical Interface

Ascent IIV comes with a powerful integrated graphical interface. With a few mouse clicks, it directs users to the RTL source code that caused the problem and the VCD proof for Undesired Sequence Checks. The graphical debugger is designed to enable users to start at the highest level of the problem description and to push deeper until the root cause is isolated. Ascent IIV supports Springsoft Verdi interface and OEM versions are available direct from Real Intent.

